PROGRAMMABLE NON-INTEGER FRACTIONAL DIVIDER

Abstract

A non-integer fractional divider is disclosed. According to the present invention, the non-integer fractional divider comprises means for dividing a reference clock signal having a period 'P' by a non-integer ratio 'K'. In a preferred embodiment, the divider comprises means for receiving a plurality 'N' of clock signals issued from the reference clock signal and wherein each clock signal is equally phase shifted by a 'P/N' delay one over the other. Selection means are coupled to the receiving means for selecting a first and a second clock signals between the plurality 'N' of clock signals. The selected clock signals are such that the phase shift delay between the two selected clock signals is representative of the non-integer value of the ratio 'K'. The selected clock signals are combined into combining means to generate a clock signal being phase shifted by the non-integer part of the non-integer ratio. Then, dividing means are coupled to the combining means for dividing the shifted clock signal by the integer part of the non-integer ratio.